Victor Yuan

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Lab – Logic gates

Introduction

The goal of this experiment is to demonstrate how a logical Gate works. If shows the threshold voltage of when a hex invertor (NOT Gate) and a AND logic gates switches from logical 1 to 0 and 0 to 1.

Team Member Responsibilities

This Lab was done alone.

Materials:

ELENCO Digital Analog kit Digital multi-meter TTL 7404 hex inverter chip

HP E3631A Triple Output DC Power Supply TTL 7408 quad AND chip

Procedure

In experiment one, a LED light on the ELENCO Digital Analog Trainer kit was connected to a power source. The input voltages ranged from 0 to 5v at increments of 0.2 volts. The brightness of the LED was recorded as either none, low, medium, or high.

In experiment two, six different logic gates on the ELENCO Digital Analog Trainer kit was connected, separately (one at a time) to a multi-meter. The voltage output for each of the logical 0 and 1 for each gate was recorded.

In experiment three, a 7404 hex inverter chip was placed in the middle of the breadboard on the ELENCO Digital Analog Trainer kit. The chip has an independent power supply. An input voltage from a power source varied from 0 to 5v by increments of 0.2v. The output voltage was measured by the multi-meter and recorded at each increment. All equipment had the same ground.

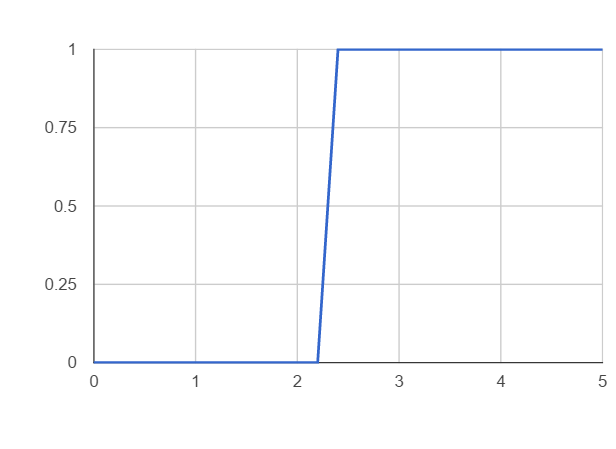
In experiment four the power supply to the chip in experiment 3 was cut off to see the output when there is no input.

In experiment five a 7408 AND Gate chip was placed in the middle of the breadboard on the ELENCO Digital Analog Trainer kit. The chip has an independent power supply. Two input voltage from a power source varied between 0 to 5v. The output was a LED light bulb and whether if the light bulb was on or off was measured. All equipment had the same ground.

In experiment six, one of the input voltage was unplugged while the LED light was measured. This was repeated in reverse with the second voltage, and the LED was measured again.

1. Experiment 1:

|  |  |  |
| --- | --- | --- |
| experiment 1 |  |  |
| input (volts) | luminosity | Logical |
| 0 | none | 0 |
| 0.2 | none | 0 |
| 0.4 | none | 0 |
| 0.6 | none | 0 |
| 0.8 | none | 0 |
| 1 | none | 0 |
| 1.2 | none | 0 |
| 1.4 | low | undetermined |
| 1.6 | low | undetermined |
| 1.8 | med | undetermined |
| 2 | med | undetermined |
| 2.2 | med | undetermined |
| 2.4 | high | 1 |
| 2.6 | high | 1 |
| 2.8 | high | 1 |
| 3 | high | 1 |
| 3.2 | high | 1 |
| 3.4 | high | 1 |
| 3.6 | high | 1 |
| 3.8 | high | 1 |
| 4 | high | 1 |
| 4.2 | high | 1 |
| 4.4 | high | 1 |
| 4.6 | high | 1 |
| 4.8 | high | 1 |
| 5 | high | 1 |



Data:

1. Can the LED be used to accurately determine the logical value of a properly operating TTL logic gate? Be sure to consider both input and output voltage ranges. If so, how?

Yes, by setting the voltage to be 0 to 1.2v the light will be off therefore a 0 is the return value, by setting the voltage to be between 2.4 and 5v the light will on therefore a 1 is the return value.

2. Can the LED be used to accurately determine a TTL logic signal in the indeterminate range? If so, how?

No because it is unclear if it’s on or not, hence the name “indeterminate”.

II. Experiment 2:

Data:

|  |  |  |  |
| --- | --- | --- | --- |
| experiment 2 |  |  |  |
|  | gate #0 |  |  |
| Logical | 0 | 0.231 | mV |
| Logical | 1 | 4.9556 | V |
|  | gate #1 |  |  |
| Logical | 0 | 0.237 | mV |
| Logical | 1 | 4.9555 | V |
|  | gate #2 |  |  |
| Logical | 0 | 0.224 | mV |
| Logical | 1 | 4.9555 | V |
|  | gate #3 |  |  |
| Logical | 0 | 0.219 | mV |
| Logical | 1 | 4.9555 | V |
|  | gate #4 |  |  |
| Logical | 0 | 0.214 | mV |
| Logical | 1 | 4.9555 | V |
|  | gate #5 |  |  |
| Logical | 0 | 0.211 | mV |
| Logical | 1 | 4.9555 | V |
|  | gate #6 |  |  |
| Logical | 0 | 0.217 | mV |
| Logical | 1 | 4.9555 | V |

1. Can a switch on an ELENCO Digital Analog Trainer kit be used to accurately generate a logical 0 and 1? If so, how?

Yes, it generates around 0.220 mV for logical 0, and it generates around 4.95v for logical 1. The indicator for logical 0 and 1 is a LED light.

III. Experiment 3:

Data:

|  |  |
| --- | --- |
| experiment 3 |  |
| input voltage(volts) | output voltage(volts) |
| 0 | 4.2743 |
| 0.2 | 4.1974 |
| 0.4 | 4.0691 |
| 0.6 | 3.9446 |
| 0.8 | 3.8145 |
| 1 | 1.2467 |
| 1.2 | 0.14529 |
| 1.4 | 0.1452 |
| 1.6 | 0.14488 |
| 1.8 | 0.14533 |
| 2 | 0.14463 |
| 2.2 | 0.14637 |
| 2.4 | 0.14637 |
| 2.6 | 0.14637 |
| 2.8 | 0.14637 |
| 3 | 0.14637 |
| 3.2 | 0.14637 |
| 3.4 | 0.14637 |
| 3.6 | 0.14637 |
| 3.8 | 0.14637 |
| 4 | 0.14637 |
| 4.2 | 0.14637 |
| 4.4 | 0.14637 |
| 4.6 | 0.14637 |
| 4.8 | 0.14637 |
| 5 | 0.14637 |

1. Does the 7404 hex inverter follow the convention relating voltage levels of a TTL logic signal to the abstract logical values of 0 and 1?

It follows the same pattern however the results are inverted, lower voltages are used for logical 1 and higher voltages are used for logical 0, so no it does not follow conventional voltage levels.

1. Does the 7404 hex inverter correctly realize the abstract NOT logical function?

Yes it does.

IV. Experiment 4:

Data:

|  |  |
| --- | --- |
| experiment 4 |  |
| input (volts) | out (volts) |
| 1.2564 | 0.14197 |

1. Does an unterminated input of a 7404 hex inverter act as a logical 0 or 1?

The output is .014197v which means the light was off, therefore logical 0.

V. Experiment 5:

Data:

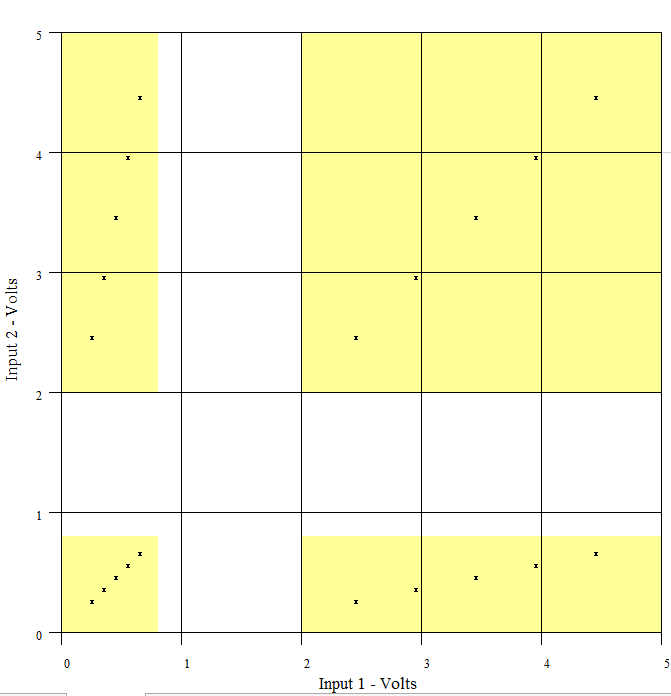
|  |  |  |  |
| --- | --- | --- | --- |
| experiment 5 |  |  |  |
| input 1(volts) | input 2(volts) | light bulb | Logical |
| 0.3 | 0.3 | off | 0 |
| 0.4 | 0.4 | off | 0 |
| 0.5 | 0.5 | off | 0 |
| 0.6 | 0.6 | off | 0 |
| 0.7 | 0.7 | off | 0 |
| 0.3 | 2.5 | off | 0 |
| 0.4 | 3 | off | 0 |
| 0.5 | 3.5 | off | 0 |
| 0.6 | 4 | off | 0 |
| 0.7 | 4.5 | off | 0 |
| 2.5 | 0.3 | off | 0 |
| 3 | 0.4 | off | 0 |
| 3.5 | 0.5 | off | 0 |
| 4 | 0.6 | off | 0 |
| 4.5 | 0.7 | off | 0 |
| 2.5 | 2.5 | on | 1 |
| 3 | 3 | on | 1 |
| 3.5 | 3.5 | on | 1 |
| 4 | 4 | on | 1 |
| 4.5 | 4.5 | on | 1 |
| 5 | 5 | on | 1 |

1. Does the 7408 quad AND gate follow the convention relating TTL logic input voltage levels to the abstract output logical values of 0 and 1?

Yes even without the usual undetermined values. Before we were determining if a light was on or not by examining the dimness, there is no undetermined values because when it is undetermined the and logic assumes 0 and 0 AND’ed with 0 or a 1 automatically becomes 0.

1. Does the 7408 quad AND gate correctly realize the abstract AND logical function?

Yes when both inputs are around 3v olts logical 1 is interpreted and then a logical 1 is passed on.



VI. Experiment 6:

Data:

|  |  |  |  |
| --- | --- | --- | --- |
| experiment 6 |  |  |  |
| input 1(volts) | input 2(volts) |  |  |
| 1.3584 | 1.5069 | on | 1 |
| 1.358 | 1.3604 | on | 1 |

1. Does an unterminated input of a 7408 quad AND gate act as a logical 0 or 1?

Based on the gathered data it acts as a logical 1

VII. Conclusions:

1. Discuss how 7400 family TTL logic gates can be used to implement abstract logical functions.

The 7404 hex inverter is equivalent to the compliment operation. This inverter can be used to flip 0 to 1 or 1 to 0.

The 7408 quad AND gate is the AND operation. This logic gate can be used to check if both conditions are checked before releasing voltage for 1

1. Discuss why the permissible input voltage range fully contains the guaranteed output voltage range for a given logical value.

While it might not matter for a single Logical gate to have equal input and output ranges in more complex wiring like a transistor having a different range of voltage input output would cause errors its best to set a standard across all logical gates.

Conclusion the goal of understanding voltage thresholds for logic gates AND and NOT of the TTL was met.